Abstract

A network processor or other type of processor includes first classification circuitry, scheduling circuitry and second classification circuitry. The first classification circuitry is configured to determine for a given packet received by the processor whether the packet has one or more errors. The scheduling circuitry in an illustrative embodiment receives an indication of the error determination made by the first classification circuitry, and based on the indication controls the dropping of the given packet from the processor memories if the packet has one or more errors, e.g., via a flush transmit command. The second classification circuitry, which may be implemented as a single classification engine or a set of such engines, may be configured to perform at least one classification operation for the given packet, e.g., if the packet is supplied thereto by the scheduling circuitry. Particular classification operations performed by at least one of the first and second classification circuitry are programmable via software that may be supplied to the processor via an associated host device. The processor may be configured as a network processor integrated circuit to provide an interface between a network and a switch fabric in a router or switch.